FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
112740-219	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	
09/890433	
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE
PCT/DE00/00176	21 January 2000
PRIORITY DATE CLAIMED	
28 January 1999	

TITLE OF INVENTION
METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS

APPLICANT(S) FOR DO/EO/US
Athanase Mariggis

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☒ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Submission of Drawings Figure s 1-5 on five sheets

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/890433	PCT/DE00/00176	112740-219

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1,000.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	**$860.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$710.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$690.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	6 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $80.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$860.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**. ☐				**$0.00**	
SUBTOTAL =				**$860.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$860.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$860.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$860.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **02-1818** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

William E. Vaughan (Reg. No. 39,056)
Bell, Boyd & Lloyd LLC
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Chicago, Illinois 60690

SIGNATURE

William E. Vaughan
NAME

39,056
REGISTRATION NUMBER

July 30, 2001
DATE

BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY-CHAPTER II

PRELIMINARY AMENDMENT

APPLICANT: Athanase Mariggis DOCKET NO: 112740-219

SERIAL NO: GROUP ART UNIT:

EXAMINER:

INTERNATIONAL APPLICATION NO: PCT/DE00/00176

INTERNATIONAL FILING DATE: 21 January 2000

INVENTION: METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Please amend the above-identified International Application before entry into the National stage before the U.S. Patent and Trademark Office under 35 U.S.C. §371 as follows:

In the Specification:

Please replace the Specification of the present application, including the Abstract, with the following Substitute Specification:

SPECIFICATION

TITLE

METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for converting NxSTM-1 signals into STM-N signals, wherein the STM-N signals are split into N STM-1 signals which are sent via different paths and can be regenerated and forwarded in a practical manner at a receiving end.

Description of the Prior Art

As a rule, contemporary transmission methods are subdivided into transmission methods which transmit information in accordance with a synchronous transfer mode (STM) or an asynchronous transfer mode (ATM).

The synchronous transfer mode (STM) is based on the transmission of information in SDH (Synchronous Digital Hierarchy) transmission technology. In this technology, the information is transmitted in frames. These are subdivided into a control field (SOH, Section Overhead; POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted while in the latter, payload is deposited. The payload used can also be ATM cells. These must then be arranged in the frame structure at the beginning of the transmission process and removed again at the receiving end. The control information considered is, for example, information with respect to the security of the transmission, bit errors, circuit failure, clock accuracy, etc.

The control field has two sub-areas SOH and POH. The sub-area designated by SOH has control information with respect to a transmission section (for example between two switching systems) whereas in the sub-area designated by POH, control information is transmitted between two subscribers (end-to-end).

The transmission of information via the SDH transmission technology assumes high clock accuracy. If clock inaccuracies occur during the transmission process, for example due to delay fluctuations, or if different clock rates are defined due to different situations in different countries, the received containers become displaced beyond the frames. A frame can, therefore, still contain part of the payload of the last container and part of its own container.

In contemporary synchronous transmission systems, STM-1 interfaces are used. An STM-1 interface is physically represented by a connection between two SDH switching systems. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching networks arranged in the SDH switching system are currently designed for switching through STM-1 signals in the prior art.

In the future, however, higher-order signals such as STM-N (N>1) signals are to be transmitted. This results in circuit switching problems in the known SDH switching networks used. A method for bypassing these problems, known in the prior art, is the Virtual Concatenation Mode. This is a standardized method by means of via which, for example, STM-4 signals are split into 4 STM-1 signals. During the transmission, 4 STM-1 signals are thus supplied to the receiving switch, switched through and then assembled again to form one STM-4 signal.

In this process, however, the NxSTM-1 signals pass through different paths in the network. Although the NxSTM-1 signals are sent out at the same time, they arrive at different times at the receiving switching center due to different delays. Converting the STM-1 signals into NxSTM-1 signals, however, requires that the STM-1 signals arrive at the same time. In the prior art, storage devices such as, for example, FIFO storage devices are used for recovering the containers in the correct order in order to solve this problem. For this purpose, the FIFO storage devices must be addressed absolutely which means resulting in increased expenditure since, on the one hand, the absolute addresses must always be stored somewhere, and on the other hand, a +/- area must be reserved. In practice, this is associated with increased control expenditure.

The present invention is, therefore, directed to an approach to have the STM-1 signals sent via different paths which can be regenerated and forwarded in a practical manner at the receiving end.

SUMMARY OF THE INVENTION

Accordingly, an advantageous factor in the present invention is, in particular, a relative dynamic logic operation between write addresses and read addresses of the FIFO storage devices. This renders superfluous a continuous absolute control of the write and read addresses respectively. Furthermore, such a procedure is associated with a gain in dynamic range during the conversion process.

Accordingly, in an embodiment of the present invention, a method is provided for converting NxSTM-1 signals into STM-N signals which includes the steps of: providing a number of STM-1 signals which respectively have a first

control field, a second control field and a payload field filled with payload, the beginning of the payload field being defined by a marker, the payload field including a number of interface devices which respectively include a store and which are used for accommodating the number of STM-1 signals; storing the respective payload of the STM-1 signals in a cyclic order in the store of the respectively associated interface device at a right address corresponding to a number of payload data which have arrived; forming a relative address with respect to the markers which have arrived based on the marker which arrived last; and removing, at the relative address formed, the payload again from the stores of the respectively associated interface device in the same cyclic order as during the right process in supplying the payload to an STM-N frame as of out put data.

In an embodiment, the method further includes the steps of forming the right address in the store by incrementing in a first counting device as determined by the number of payload data that have arrived, until one of the first control field and the second control field is detected, and transferring the count of the first counting device to the store.

In an embodiment, the method further includes the steps of counting the payload data in a second counting device from an instant when the second control field is detected until a time when all markers have arrived, forming a difference between the counts of the first and second counting devices, decrementing the difference by one, and transferring the decremented value calculated as read address to a third counting device at which the payload stored in the store is removed.

In an embodiment of the method, the store is constructed as a cyclic random-access circular buffer.

In an embodiment of the method, the interface devices are synchronized within one-half period of a VC-4 container.

In an embodiment of the method, the interface devices are synchronized outside the half period of the VC-4 container by combining the pointers of at least two VC-4 containers until a synchronization circuit which follows the interface devices and determines structured payload data acquires lock.

Additional features and advantages of the present invention are described in, and will be apparent from, the following detailed description of the preferred embodiment and the drawings.

DESCRIPTION OF THE DRAWINGS

Figure 1 shows an SDH container as known in the prior art;

Figure 2 shows the container of an STM-4 interface;

Figure 3 shows a circuit arrangement on which the method according to the present invention is running;

Figure 4 shows the reading of the payload from the FIFO storage devices according to the method of the present invention; and

Figure 5 shows the markers arriving at different times in the FIFO storage devices.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows the structure of an SDH transmission frame. Accordingly, two SDH frames F_1, F_2 are shown as examples. The control information is deposited in the control fields SOH, POH. The payload is transmitted in a container CON. According to the exemplary embodiment above, this is intended to be a virtual container VC-4 wherein the payload transmitted here is transmitted at a payload bit rate of 149 Mbit/s.

A frame is built up of a total of 9 rows. The control field SOH has a width of 9 bytes per row. The container CON exhibits a width of 260 bytes per row and the control field POH has 1 byte per row. Overall, this results in a magnitude of 2,430 bytes (9x(9+1+260)), for one SDH frame, 2340 bytes being provided for transmitting payload.

The start of the container CON in the relevant frame is designated by a marker J_1. The position of the marker J_1 is stored in a special pointer field H_1, H_2, H_3 of the control field SOH which forms a pointer. This pointer points to the position of the marker J_1. The control information deposited in the control field SOH is always deposited at the same place. The container CON can migrate beyond the frame boundaries F_1, F_2 due to clock inaccuracies. The same applies to

the control field POH as well. In Figure 1, the marker J_1 marks the start of the container CON of the frame F_1. The start of the container of the frame F_2 is defined by another marker J_1 of frame F_2. Thus, the payload contained in the container of frame F_1 is also part of frame F_2 beyond the frame boundaries.

Figure 2 shows the conditions for an STM-4 interface. The STM-4 signals have here been split into 4 STM-1 signals. Here, too, the containers migrate beyond frame boundaries due to clock inaccuracies. The beginning of the individual containers is shown by 4 J_1 pointers belonging to the frames F_1...F_4 in Figure 2. The origin of this is that, although the 4 STM-1 signals have been sent out at the same time, they have experienced delay differences along the respective paths. For this reason, these signals also have become stored in different storage areas of the FIFO-type buffer stores. Converting the 4 STM-1 signals back into one STM-4 signal requires time-synchronous conversion since only this ensures the STM-4 signal.

Figure 3 discloses a circuit arrangement by which the restoration of an STM-4 signal from 4 STM-1 signals is achieved. Accordingly, 4 interface devices P_0...P_3 are shown. Each of these 4 interface devices P_0...P_3 is used at the receiving end to terminate the connecting line via which the STM-1 signal is transmitted in each case. Since the control data transmitted in the control fields SOH, POH are specific to STM-1, this information must be suppressed during the conversion into an STM-4 signal.

At the input end, the 4 interface devices P_0...P_3 are supplied with the STM-1 signals Data_in0...Data_in3. The interface device P_0 is thus supplied with the STM-1 signals Data_in0, the interface device P_1 is supplied with the STM-1 signals Data_in1, etc. These STM-1 signals are then checked to see whether the incoming information is payload or control information. In the control field SOH, an alignment word is also transmitted to which the frame synchronizes in each case. If this alignment word is received, a signal SOH_disable is activated and supplied to the relevant interface device. The third word in the control field SOH is a pointer

which points to the marker J_1. If this is detected, a signal POH_disable is activated and supplied to the relevant interface device.

Furthermore, each of the 4 interface devices $P_0..P_3$ has a cyclic circular buffer R. This is constructed as Random Access Memory (RAM) and has the function of a FIFO store. As a rule, this circular buffer R is worth, in each case, 1170 bytes as one half of a container CON. Furthermore, a counter AWC in which the payload bytes are counted as determined by the state of the signal SOH_disable, is in each case, provided in each of the interface devices. When both signals SOH_disable, POH_disable are inactive, this count is read out and supplied to the circular buffer R via a signal addr_in. At the same time, a signal write_enable is supplied. The count of the counter AWC thus reproduces the memory address in the circular buffer R at which the relevant payload bytes are stored. Furthermore, a counter PC which is incremented by the incoming payload bytes on detection of the marker J_1 is provided in each of the 4 interface devices $P_0...P_3$. In a further counter ARC, which is also arranged in each of the 4 interface devices $P_0...P_3$, the address of the circular buffer R under which the payload bytes are read out again is stored as determined by the count of the counter AWC, PC.

The devices PD, RC are used as higher-level devices of the 4 interface devices $P_0...P_3$. The former is a monitoring device which determines whether the markers J_1 of all four interface devices $P_0...P_3$ have been detected. The device RC is a higher-level control logic which controls and monitors the read processes.

In the text which follows, the operation of the circuit will be briefly explained:

The STM-1 signals data_in0...data_in3 are accepted by the relevant interface device. If the signal SOH_disable is inactive, the counter AWC activates a signal write_enable. At the same time, the counter AWC is incremented by the number of incoming payload bytes. The value obtained in this manner is supplied to the circular buffer R via a signal addr_in and is interpreted as address by the buffer. The data data_in are deposited in the circular buffer R as determined by this address. Due to the logical OR operation on the signals SOH_disable,

POH_disable (write_enable), only payload is transferred into the circular buffer R. The information stored in the control fields SOH, POH is thus suppressed.

On start-up, the signals POH_J_1 of all interface devices P_0...P_3 are set to "0". If the signaling signal for the marker J_1 of the relevant interface device is detected, the counter PC is started by the signal POH_disable. The signal POH_J_1 of the corresponding interface device is then set to a logical "1" or "high". As long as the signal POH_J_1 assumes the state of logical "1", the payload bytes are counted. If the markers J_1 have been received by all interface devices P_0...P_3, all signals POH_J_1 are then set to a logical "1". As a result, the monitoring device PD initiates logic operations and forms the difference between the counts AWC and PC, decremented by 1 and loaded into the counter ARC. The monitoring device PD then sets all signals POH_J_1 to 0 for the next cycle. Furthermore, if the counts of the counters AWC and ARC are equal, the read process is stopped in all interface devices and a signal disable_read is generated because there is no payload in the circular buffer R in at least one of the interface devices P_0...P_3.

In detail, the following procedure is adopted:

The counts of counters AWC and PC are determined. The difference between the two counts is decremented by 1 and the result is stored in the counter ARC. At the instant at which all markers J_1 have arrived, the relative delay difference of the STM-1 signals with respect to the STM-1 signals which have arrived last is, thus, given in the counter PC.

The counters ARC of all interface devices are then triggered to transfer the content to the circular buffer R via, in each case, one signal addr_out. The latter interprets this value as an address. The data stored under this address are read out and forwarded as STM-4 signal as output data data_out.

The corresponding conditions are reproduced in Figure 4. Accordingly, the 4 cyclic circular buffers R of the 4 interface devices R(P_0)...R(P_3) are shown. As a last marker, marker J_1 of the interface devices P_1 has arrived, for example. All counters are then stopped. Subsequently, the relative address to the markers J_1 which are stored in the remaining 3 interface devices is then formed. In the case of

the interface devices R(P_0) the difference is 6 payload bytes. In the case of the interface device P_2, the difference is 8 payload bytes and in the case of the interface device P_3, the difference is 17 payload bytes. Triggering the higher-level logic device RC, the payload is read out and supplied to an STM-4 frame FR which regenerates 1 STM-4 signal from the 4 STM-1 signals.

The precondition for this method is that the markers J_1 of all STM-1 signals arrive within a half VC-4 period. The corresponding conditions are shown for the example of 4 STM-1 signals in Figure 2. The markers J_1 are placed within the VC-4 period. For this reason, the interface circuits can synchronize without additional signal evaluation. For example, marker J_1 of frame F_3 of interface device P_3 arrives first, for example, as described for Figure 2. The counter PC is then started and counts up to 1170. If no further markers J_1 of the remaining containers CON are detected until then, all counters PC and all signals POH_J_1 are reset and synchronization recommences correctly with marker J_1 of frame F_1 at the next cycle.

According to the present exemplary embodiment, it has been assumed that the magnitude of the delay differences is smaller than one half container period of a virtual VC-4 container. However, delay differences greater than one half container period of a virtual VC-4 container can also be treated with a modification of the method.

The interface device according to Figure 3 can still synchronize if the payload in the container is structured. In this case, the circular buffer R must be enlarged in accordance with the greatest delay to be expected. The corresponding conditions are shown in Figure 5. This is the case, for example, if the payload consists of ATM cells, frame relay or TCP/IP data. Because of such transmission formats, synchronization can be carried out because error-free transmission is detected by the control field SOH and, in this case, the header of the cell is detected and evaluated by an additional payload synchronization circuit corresponding to the transmission format. The synchronization circuit is designated by HSC in Figure 5. The synchronization can be restored by combining the pointers of 2 or more VC-4

containers (4 pointers in the case of STM-4) until the payload synchronization circuit HSC acquires lock. The combination can be obtained from a simple addition of 2340 bytes in the counting devices of the counters ARC, triggered by a device J_1CL (J_1 combining logic) since, when a number of markers J_1 is found, the frame to which this marker belongs cannot be reliably detected. The difference between 2 markers J_1 of the same interface device is 2340 payload bytes. After the payload synchronization circuit HSC has acquired lock, the markers J_1 will not be combined because only jumps of 3 bytes are allowed according to the SDH standard, unless the system is re-initialized.

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

ABSTRACT OF THE DISCLOSURE

During the transmission of SDH signals, higher-order signals such as STM-N (N>1) signals are transmitted. To prevent circuit switching problems in the known STM-1 switching networks used, the STM-N signals are split into N STM-1 signals in accordance with the known virtual concatenation mode. These signals, however, pass through different paths in the network which leads to different delays. The present invention solves these problems by addressing FIFO storage devices with relative addressing at the receiving end in order to read out the payload data stored there.

In the claims:

On page 11, cancel line 1, and substitute the following left-hand justified heading therefor:

I Claim as My Invention:

Please cancel 1-6, without prejudice, and substitute the following claims therefor:

7. A method for converting NxSTM-1 signals into STM-N signals, the method comprising the steps of:

providing a plurality of STM-1 signals which respectively have a first control field, a second control field, and a payload field filled with payload, the beginning of the payload field being defined by a marker, the payload field including a plurality of interface devices which respectively include a store and which are used for accommodating the plurality of STM-1 signals;

storing the respective payload of the plurality of STM-1 signals in a cyclic order in the store of the respectively associated interface device at a right address corresponding to a number of payload data which have arrived;

forming a relative address with respect to the markers which have arrived based on the marker which arrived last; and

removing, at the relative address formed, the payload again from the stores of the respectively associated interface device in the same cyclic order as during the right process and supplying the payload to an STM-N frame as output data.

8. A method for converting NxSTM-1 signals into STM-N signals as claimed in claim 7, the method further comprising the steps of:

forming the right address in the store by incrementing in a first counting device as determined by the number of payload data that have arrived, until one of the first control field and the second control field is detected; and

transferring the count of the first counting device to the store.

9. A method for converting NxSTM-1 signals into STM-N as claimed in claim 7, the method further comprising the steps of:

counting the payload data in a second counting device from an instant when the second control field is detected until a time when all markers have arrived;

forming a difference between the counts of the first and second counting devices;

decrementing the difference by one; and

transferring the decremented value calculated as read address to a third counting device at which the payload stored in the store is removed.

10. A method for converting NxSTM-1 signals into STM-N signals as claimed in claim 7, wherein the store is constructed as a cyclic random-access circular buffer.

11. A method for converting NxSTM-1 signals into STM-N signals as claimed in claim 7, wherein the interface devices are synchronized within one-half period of a VC-4 container.

12. A method for converting NxSTM-a signals into STM-N signals as claimed in claim 7, wherein the interface devices are synchronized outside one-half period of a VC-4 container by combining the pointers of at least two VC-4 containers until a synchronization circuit which follows the interface devices and determines structured payload data acquires lock.

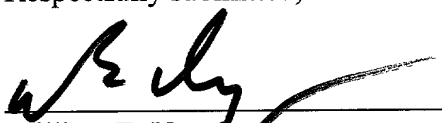
REMARKS

The present amendment makes editorial changes and corrects typographical errors in the specification, which includes the Abstract, in order to conform the specification to the requirements of United States Patent Practice. No new matter is added thereby. Attached hereto is a marked-up version of the changes made to the specification by the present amendment. The attached page is captioned "**Version With Markings To Show Changes Made**".

In addition, the present amendment cancels original claims 1-6 in favor of new claims 7-12. Claims 7-12 have been presented solely because the revisions by crossing-out and underlining which would have been necessary in claims 1-6 in order to present those claims in accordance with preferred United States Patent Practice would have been too extensive, and thus would have been too burdensome. The present amendment is intended for clarification purposes only and not for substantial reasons related to patentability pursuant to 35 U.S.C. §§103, 102, 103 or 112. Indeed, the cancellation of claims 1-6 does not constitute an intent on the part of the Applicants to surrender any of the subject matter of claims 1-6.

Early consideration on the merits is respectfully requested.

Respectfully submitted,



(Reg. No. 39,056)

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Chicago, Illinois 60690-1135
(312) 807-4292
Attorneys for Applicants

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

The Specification of the present application, including the Abstract, has been amended as follows:

SPECIFICATION

TITLE

~~Description~~

~~Method for converting NxSTM-1 signals into STM-N signals~~

METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for converting NxSTM-1 signals into STM-N signals, wherein the STM-N signals are split into N STM-1 signals which are sent via different paths and can be regenerated and forwarded in a practical manner at a receiving end.

Description of the Prior Art

~~The invention relates to a method according to the preamble of claim 1.~~ As a rule, contemporary transmission methods are subdivided into transmission methods which transmit information in accordance with a synchronous transfer mode (STM) or an asynchronous transfer mode (ATM).

The synchronous transfer mode (STM) is based on the transmission of information in SDH (Synchronous Digital Hierarchy) transmission technology. In this technology, the information is transmitted in frames. These are subdivided into a control field (SOH, Section Overhead; POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted ~~whilst~~ while in the latter, payload is deposited. The payload used can also be ATM cells. These must then be arranged in the frame structure at the beginning of the transmission process and removed again at the receiving end. The control

information considered is, for example, information with respect to the security of the transmission, bit errors, circuit failure, clock accuracy, etc.

The control field has two sub-areas SOH and POH. The sub-area designated by SOH has control information with respect to a transmission section (for example between two switching systems) whereas in the sub-area designated by POH, control information is transmitted between two subscribers (end-to-end).

The transmission of information ~~by means of~~ via the SDH transmission technology assumes high clock accuracy. If clock inaccuracies occur during the transmission process, for example due to delay fluctuations, or if different clock rates are defined due to different situations in different countries, the received containers become displaced beyond the frames. A frame can, therefore, still contain part of the payload of the last container and part of its own container.

In contemporary synchronous transmission systems, STM-1 interfaces are used. An STM-1 interface is physically represented by a connection between two SDH switching systems. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching networks arranged in the SDH switching system are currently designed for switching through STM-1 signals in the prior art.

In the future, however, higher-order signals such as STM-N (N>1) signals are to be transmitted. This results in circuit switching problems in the known SDH switching networks ~~hitherto~~ used. A method for bypassing these problems, known in the prior art, is the Virtual Concatenation Mode. This is a standardized method ~~by means of~~ via which, for example, STM-4 signals are split into 4 STM-1 signals. During the transmission, 4 STM-1 signals are ~~thus~~ supplied to the receiving switch, switched through and then assembled again to form one STM-4 signal.

In this process, however, the NxSTM-1 signals pass through different paths in the network. Although the NxSTM-1 signals are sent out at the same time, they arrive at different times at the receiving switching center due to different delays. Converting the STM-1 signals into NxSTM-1 signals, however, requires that the STM-1 signals arrive at the same time. In the prior art, storage devices such as, for

example, FIFO storage devices are used for recovering the containers in the correct order in order to solve this problem. For this purpose, the FIFO storage devices must be addressed absolutely ~~which means~~ resulting in increased expenditure since, on the one hand, the absolute addresses must always be stored somewhere, and on the other hand, a +/- area must be reserved. In practice, this is associated with increased control expenditure.

The present invention is, therefore, directed to ~~based on the object of demonstrating~~ an approach to have the STM-1 signals sent via different paths which can be regenerated and forwarded in a practical manner at the receiving end.

~~The invention is achieved by the features specified in the characterizing clause on the basis of the features specified in the preamble of claim 1.~~

SUMMARY OF THE INVENTION

Accordingly, an ~~The~~ advantageous factor in the present invention is, in particular, a relative dynamic logic operation between write addresses and read addresses of the FIFO storage devices. This renders superfluous a continuous absolute control of the write and read addresses respectively. Furthermore, such a procedure is associated with a gain in dynamic range during the conversion process.

Accordingly, in an embodiment of the present invention, a method is provided for converting NxSTM-1 signals into STM-N signals which includes the steps of: providing a number of STM-1 signals which respectively have a first control field, a second control field and a payload field filled with payload, the beginning of the payload field being defined by a marker, the payload field including a number of interface devices which respectively include a store and which are used for accommodating the number of STM-1 signals; storing the respective payload of the STM-1 signals in a cyclic order in the store of the respectively associated interface device at a right address corresponding to a number of payload data which have arrived; forming a relative address with respect to the markers which have arrived based on the marker which arrived last; and removing, at the relative address formed, the payload again from the stores of the

respectively associated interface device in the same cyclic order as during the right process in supplying the payload to an STM-N frame as of out put data.

In an embodiment, the method further includes the steps of forming the right address in the store by incrementing in a first counting device as determined by the number of payload data that have arrived, until one of the first control field and the second control field is detected, and transferring the count of the first counting device to the store.

In an embodiment, the method further includes the steps of counting the payload data in a second counting device from an instant when the second control field is detected until a time when all markers have arrived, forming a difference between the counts of the first and second counting devices, decrementing the difference by one, and transferring the decremented value calculated as read address to a third counting device at which the payload stored in the store is removed.

In an embodiment of the method, the store is constructed as a cyclic random-access circular buffer.

In an embodiment of the method, the interface devices are synchronized within one-half period of a VC-4 container.

In an embodiment of the method, the interface devices are synchronized outside the half period of the VC-4 container by combining the pointers of at least two VC-4 containers until a synchronization circuit which follows the interface devices and determines structured payload data acquires lock.

Additional features and advantages of the present invention are described in, and will be apparent from, the following detailed description of the preferred embodiment and the drawings.

~~Advantageous further developments of the invention are specified in the subclaims.~~

~~In the text which follows, the invention will be explained in greater detail with reference to an exemplary embodiment. In the figures:~~

DESCRIPTION OF THE DRAWINGS

Figure 1 shows an SDH container ~~according to~~ as known in the prior art;

Figure 2 shows the container of an STM-4 interface;

Figure 3 shows a circuit arrangement on which the method according to the present invention is running;

Figure 4 shows the reading of the payload from the FIFO storage devices according to the method ~~according to~~ of the present invention; and

Figure 5 shows the markers arriving at different times in the FIFO storage devices.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows the structure of an SDH transmission frame. Accordingly, two SDH frames F_1, F_2 are shown as examples. The control information is deposited in the control fields SOH, POH. The payload is transmitted in a container CON. According to the exemplary embodiment above, this is intended to be a virtual container VC-4. ~~This means that~~ wherein the payload transmitted here is transmitted at a payload bit rate of 149 Mbit/s.

A frame is built up of a total of 9 rows. The control field SOH has a width of 9 bytes per row. The container CON exhibits a width of 260 bytes per row and the control field POH has 1 byte per row. Overall, this results in a magnitude of 2,430 bytes (9x(9+1+260)), for one SDH frame, 2340 bytes being provided for transmitting payload.

The start of the container CON in the relevant frame is designated by a marker J_1. The position of the marker J_1 is stored in a special pointer field H_1, H_2, H_3 of the control field SOH which forms a pointer. This pointer points to the position of the marker J_1. The control information deposited in the control field SOH is always deposited at the same place. The container CON can migrate beyond the frame boundaries F_1, F_2 due to clock inaccuracies. The same ~~thus also~~ applies to the control field POH as well. In ~~f~~Figure 1, the marker J_1 marks the start of the container CON of the frame F_1. The start of the container of the frame F_2 is defined by another marker J_1 of frame F_2. Thus, the payload contained in the container of frame F_1 is also part of frame F_2 beyond the frame boundaries.

Figure 2 shows the conditions for an STM-4 interface. The STM-4 signals have here been split into 4 STM-1 signals. Here, too, the containers migrate beyond frame boundaries due to clock inaccuracies. The beginning of the individual containers is shown by 4 J_1 pointers belonging to the frames F_1...F_4 in ~~f~~Figure 2. The origin of this is that, although the 4 STM-1 signals have been sent out at the same time, they have experienced delay differences along the respective paths. For this reason, these signals also have become stored in different storage areas of the FIFO-type buffer stores. Converting the 4 STM-1 signals back into one STM-4 signal requires time-synchronous conversion since only this ensures the STM-4 signal.

Figure 3 discloses a circuit arrangement by ~~means of~~ which the restoration of an STM-4 signal from 4 STM-1 signals is achieved. Accordingly, 4 interface devices P_0...P_3 are shown. Each of these 4 interface devices P_0...P_3 is used at the receiving end to terminate the connecting line via which the STM-1 signal is transmitted in each case. Since the control data transmitted in the control fields SOH, POH are specific to STM-1, this information must be suppressed during the conversion into an STM-4 signal.

At the input end, the 4 interface devices P_0...P_3 are supplied with the STM-1 signals Data_in0...Data_in3. The interface device P_0 is thus supplied with the STM-1 signals Data_in0, the interface device P_1 is supplied with the STM-1 signals Data_in1, etc. These STM-1 signals are then checked to see whether the incoming information is payload or control information. In the control field SOH, an alignment word is also transmitted to which the frame synchronizes in each case. If this alignment word is received, a signal SOH_disable is activated and supplied to the relevant interface device. The third word in the control field SOH is a pointer which points to the marker J_1. If this is detected, a signal POH_disable is activated and ~~this is also~~ supplied to the relevant interface device.

Furthermore, each of the 4 interface devices P_0..P_3 has a cyclic circular buffer R. This is constructed as Random Access Memory (RAM) and has the function of a FIFO store. As a rule, this circular buffer R is worth, in each case,

1170 bytes as one half of a container CON. Furthermore, a counter AWC in which the payload bytes are counted as determined by the state of the signal SOH_disable, is in each case, provided in each of the interface devices. When both signals SOH_disable, POH_disable are inactive, this count is read out and supplied to the circular buffer R via a signal addr_in. At the same time, a signal write_enable is supplied. The count of the counter AWC thus reproduces the memory address in the circular buffer R at which the relevant payload bytes are stored. Furthermore, a counter PC which is incremented by the incoming payload bytes on detection of the marker J_1 is provided in each of the 4 interface devices $P_0...P_3$. In a further counter ARC, which is also arranged in each of the 4 interface devices $P_0...P_3$, the address of the circular buffer R under which the payload bytes are read out again is stored as determined by the count of the counter AWC, PC.

The devices PD, RC are used as higher-level devices of the 4 interface devices $P_0...P_3$. The former is a monitoring device which determines whether the markers J_1 of all four interface devices $P_0...P_3$ have been detected. The device RC is a higher-level control logic which controls and monitors the read processes.

In the text which follows, the operation of the circuit will be briefly explained:

The STM-1 signals data_in0...data_in3 are accepted by the relevant interface device. If the signal SOH_disable is inactive, the counter AWC activates a signal write_enable. At the same time, the counter AWC is incremented by the number of incoming payload bytes. The value obtained in this manner is supplied to the circular buffer R via a signal addr_in and is interpreted as address by the buffer. The data data_in are deposited in the circular buffer R as determined by this address. Due to the logical OR operation on the signals SOH_disable, POH_disable (write_enable), only payload is transferred into the circular buffer R. The information stored in the control fields SOH, POH is thus suppressed.

On start-up, the signals POH_J_1 of all interface devices $P_0...P_3$ are set to "0". If the signaling signal for the marker J_1 of the relevant interface device is detected, the counter PC is started by the signal POH_disable. The signal POH_J_1 of the

corresponding interface device is then set to a logical "1" or "high". As long as the signal POH_J_1 assumes the state of logical "1", the payload bytes are counted. If the markers J_1 have been received by all interface devices P_0...P_3, all signals POH_J_1 are then set to a logical "1". As a result, the monitoring device PD initiates logic operations and forms the difference between the counts AWC and PC, decremented by 1 and loaded into the counter ARC. The monitoring device PD then sets all signals POH_J_1 to 0 for the next cycle. Furthermore, if the counts of the counters AWC and ARC are equal, the read process is stopped in all interface devices and a signal disable_read is generated because there is no payload in the circular buffer R in at least one of the interface devices P_0...P_3.

In detail, the following procedure is adopted:

The counts of counters AWC and PC are determined. The difference between the two counts is decremented by 1 and the result is stored in the counter ARC. At the instant at which all markers J_1 have arrived, the relative delay difference of the STM-1 signals with respect to the STM-1 signals which have arrived last is, thus, given in the counter PC.

The counters ARC of all interface devices are then triggered to transfer the content to the circular buffer R via, in each case, one signal addr_out. The latter interprets this value as an address. The data stored under this address are read out and forwarded as STM-4 signal as output data data_out.

The corresponding conditions are reproduced in ~~f~~Figure 4. Accordingly, the 4 cyclic circular buffers R of the 4 interface devices R(P_0)...R(P_3) are shown. As a last marker, marker J_1 of the interface devices P_1 has arrived, for example. All counters are then stopped. Subsequently, the relative address to the markers J_1 which are stored in the remaining 3 interface devices is then formed. In the case of the interface devices R(P_0) the difference is 6 payload bytes. In the case of the interface device P_2, the difference is 8 payload bytes and in the case of the interface device P_3, the difference is 17 payload bytes. Triggering the higher-level logic device RC, the payload is read out and supplied to an STM-4 frame FR which regenerates 1 STM-4 signal from the 4 STM-1 signals.

The precondition for this method is that the markers J_1 of all STM-1 signals arrive within a half VC-4 period. The corresponding conditions are shown for the example of 4 STM-1 signals in fFigure 2. The markers J_1 are placed within the VC-4 period. For this reason, the interface circuits can synchronize without additional signal evaluation. For example, marker J_1 of frame F_3 of interface device P_3 arrives first, for example, as described for fFigure 2. The counter PC is then started and counts up to 1170. If no further markers J_1 of the remaining containers CON are detected until then, all counters PC and all signals POH_J_1 are reset and synchronization recommences correctly with marker J_1 of frame F_1 at the next cycle.

According to the present exemplary embodiment, it has been assumed that the magnitude of the delay differences is smaller than one half container period of a virtual VC-4 container. However, delay differences greater than one half container period of a virtual VC-4 container can also be treated with a modification of the method.

The interface device according to fFigure 3 can still synchronize if the payload in the container is structured. In this case, the circular buffer R must be enlarged in accordance with the greatest delay to be expected. The corresponding conditions are shown in fFigure 5. This is the case, for example, if the payload consists of ATM cells, frame relay or TCP/IP data. Because of such transmission formats, synchronization can be carried out because error-free transmission is detected by the control field SOH and, in this case, the header of the cell is detected and evaluated by an additional payload synchronization circuit corresponding to the transmission format. The synchronization circuit is designated by HSC in fFigure 5. The synchronization can be restored by combining the pointers of 2 or more VC-4 containers (4 pointers in the case of STM-4) until the payload synchronization circuit HSC acquires lock. The combination can be obtained from a simple addition of 2340 bytes in the counting devices of the counters ARC_1 - triggered by a device J_1CL (J_1 combining logic) since, when a number of markers J_1 is found, the frame to which this marker belongs cannot be reliably detected. The

difference between 2 markers J_1 of the same interface device is 2340 payload bytes. After the payload synchronization circuit HSC has acquired lock, the markers J_1 will not be combined because only jumps of 3 bytes are allowed according to the SDH standard, unless the system is re-initialized.

Although the present invention has been described with reference to specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the spirit and scope of the invention as set forth in the hereafter appended claims.

~~Abstract~~

ABSTRACT OF THE DISCLOSURE

~~Method for converting NxSTM-1 signals into STM-N signals~~

During the transmission of SDH signals, higher-order signals such as STM-N (N>1) signals are transmitted. To prevent circuit switching problems in the known STM-1 switching networks ~~hitherto~~ used, the STM-N signals are split into N STM-1 signals in accordance with the known virtual concatenation mode. These signals, however, pass through different paths in the network which leads to different delays. The present invention solves these problems by addressing FIFO storage devices with relative addressing at the receiving end in order to read out the payload data stored there.

~~Figure 3~~

Description

Method for converting NxSTM-1 signals into STM-N signals

The invention relates to a method according to the preamble of claim 1.

As a rule, contemporary transmission methods are subdivided into transmission methods which transmit information in accordance with a synchronous transfer mode (STM) or an asynchronous transfer mode (ATM).

The synchronous transfer mode (STM) is based on the transmission of information in SDH (Synchronous Digital Hierarchy) transmission technology. In this technology, the information is transmitted in frames. These are subdivided into a control field (SOH, Section Overhead; POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted whilst in the latter, payload is deposited. The payload used can also be ATM cells. These must then be arranged in the frame structure at the beginning of the transmission process and removed again at the receiving end. The control information considered is, for example, information with respect to the security of the transmission, bit errors, circuit failure, clock accuracy, etc.

The control field has two sub-areas SOH and POH. The sub-area designated by SOH has control information with respect to a transmission section (for example between two switching systems) whereas in the sub-area designated by POH, control information is transmitted between two subscribers (end-to-end).

The transmission of information by means of the SDH transmission technology assumes high clock accuracy. If clock inaccuracies occur during the transmission process, for

example due to delay fluctuations, or if different clock rates are defined due to different situations in different countries, the received containers become displaced beyond the frames. A frame can, therefore, still contain part of the payload of the last container and part of its own container.

In contemporary synchronous transmission systems, STM-1 interfaces are used. An STM-1 interface is physically represented by a connection between two SDH switching systems. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching networks arranged in the SDH switching system are currently designed for switching through STM-1 signals in the prior art.

In future, however, higher-order signals such as STM-N (N>1) signals are to be transmitted. This results in circuit switching problems in the SDH switching networks hitherto used. A method for bypassing these problems, known in the prior art, is the Virtual Concatenation Mode. This is a standardized method by means of which, for example, STM-4 signals are split into 4 STM-1 signals. During the transmission, 4 STM-1 signals are thus supplied to the receiving switch, switched through and then assembled again to form one STM-4 signal.

In this process, however, the NxSTM-1 signals pass through different paths in the network. Although the NxSTM-1 signals are sent out at the same time, they arrive at different times at the receiving switching center due to different delays. Converting the STM-1 signals into NxSTM-1 signals, however, requires that the STM-1 signals arrive at the same time. In the prior art, storage devices such as, for example, FIFO storage devices are used for recovering the containers in the correct order in order to solve this problem. For this purpose,

the FIFO storage devices must be addressed absolutely which means increased expenditure since, on the one hand, the absolute addresses must always be stored somewhere and on the other hand a +/- area must be reserved. In practice, this is associated with increased control expenditure.

The invention is based on the object of demonstrating an approach to have the STM-1 signals sent via different paths which can be regenerated and forwarded in a practical manner at the receiving end.

The invention is achieved by the features specified in the characterizing clause on the basis of the features specified in the preamble of claim 1.

The advantageous factor in the invention is, in particular, a relative dynamic logic operation between write addresses and read addresses of the FIFO storage devices. This renders superfluous a continuous absolute control of the write and read addresses respectively. Furthermore, such a procedure is associated with a gain in dynamic range during the conversion process.

Advantageous further developments of the invention are specified in the subclaims.

In the text which follows, the invention will be explained in greater detail with reference to an exemplary embodiment. In the figures:

Figure 1 shows an SDH container according to the prior art

Figure 2 shows the container of an STM-4 interface

Figure 3 shows a circuit arrangement on which the method according to the invention is running

Figure 4 shows the reading of the payload from the FIFO storage devices according to the method according to the invention

Figure 5 shows the markers arriving at different times in the FIFO storage devices.

Figure 1 shows the structure of an SDH transmission frame. Accordingly, two SDH frames F_1, F_2 are shown as examples. The control information is deposited in the control fields SOH, POH. The payload is transmitted in a container CON. According to the exemplary embodiment above, this is intended to be a virtual container VC-4. This means that the payload transmitted here is transmitted at a payload bit rate of 149 Mbit/s.

A frame is built up of a total of 9 rows. The control field SOH has a width of 9 bytes per row. The container CON exhibits a width of 260 bytes per row and the control field POH has 1 byte per row. Overall, this results in a magnitude of 2,430 bytes (9x(9+1+260)), for one SDH frame, 2340 bytes being provided for transmitting payload.

The start of the container CON in the relevant frame is designated by a marker J_1. The position of the marker J_1 is stored in a special pointer field H_1, H_2, H_3 of the control field SOH which forms a pointer. This pointer points to the position of the marker J_1. The control information deposited in the control field SOH is always deposited at the same place. The container CON can migrate beyond the frame boundaries F_1, F_2 due to clock inaccuracies. The same thus also applies to the control field POH. In figure 1, the marker J_1 marks the start of the container CON of the frame F_1. The start of the container of the frame F_2 is defined by another marker J_1 of frame F_2. Thus, the payload contained in the container of frame F_1 is also part of frame F_2 beyond the frame boundaries.

Figure 2 shows the conditions for an STM-4 interface. The STM-4 signals have here been split into 4 STM-1 signals. Here, too, the containers migrate beyond frame boundaries due to clock inaccuracies. The beginning of the individual containers is shown by 4 J_1 pointers belonging to the frames $F_1 \ldots F_4$ in figure 2. The origin of this is that, although the 4 STM-1 signals have been sent out at the same time, they have experienced delay differences along the respective paths. For this reason, these signals also have become stored in different storage areas of the FIFO-type buffer stores. Converting the 4 STM-1 signals back into one STM-4 signal requires time-synchronous conversion since only this ensures the STM-4 signal.

Figure 3 discloses a circuit arrangement by means of which the restoration of an STM-4 signal from 4 STM-1 signals is achieved. Accordingly, 4 interface devices $P_0 \ldots P_3$ are shown. Each of these 4 interface devices $P_0 \ldots P_3$ is used at the receiving end to terminate the connecting line via which the STM-1 signal is transmitted in each case. Since the control data transmitted in the control fields SOH, POH are specific to STM-1, this information must be suppressed during the conversion into an STM-4 signal.

At the input end, the 4 interface devices $P_0 \ldots P_3$ are supplied with the STM-1 signals Data_in0...Data_in3. The interface device P_0 is thus supplied with the STM-1 signals Data_in0, the interface device P_1 is supplied with the STM-1 signals Data_in1, etc. These STM-1 signals are then checked to see whether the incoming information is payload or control information. In the control field SOH, an alignment word is also transmitted to which the frame synchronizes in each case. If this alignment word is received, a signal SOH_disable is activated and supplied to the relevant interface device. The third word in the control field SOH is a pointer which points to the

marker J_1. If this is detected, a signal POH_disable is activated and this is also supplied to the relevant interface device.

Furthermore, each of the 4 interface devices $P_0..P_3$ has a cyclic circular buffer R. This is constructed as Random Access Memory (RAM) and has the function of a FIFO store. As a rule, this circular buffer R is worth in each case 1170 bytes as one half of a container CON. Furthermore, a counter AWC in which the payload bytes are counted as determined by the state of the signal SOH_disable is in each case provided in each of the interface devices. When both signals SOH_disable, POH_disable are inactive, this count is read out and supplied to the circular buffer R via a signal addr_in. At the same time, a signal write_enable is supplied. The count of the counter AWC thus reproduces the memory address in the circular buffer R at which the relevant payload bytes are stored. Furthermore, a counter PC which is incremented by the incoming payload bytes on detection of the marker J_1 is provided in each of the 4 interface devices $P_0...P_3$. In a further counter ARC, which is also arranged in each of the 4 interface devices $P_0...P_3$, the address of the circular buffer R under which the payload bytes are read out again is stored as determined by the count of the counter AWC, PC.

The devices PD, RC are used as higher-level devices of the 4 interface devices $P_0...P_3$. The former is a monitoring device which determines whether the markers J_1 of all four interface devices $P_0...P_3$ have been detected. The device RC is a higher-level control logic which controls and monitors the read processes.

In the text which follows, the operation of the circuit will be briefly explained:

The STM-1 signals data_in0...data_in3 are accepted by the relevant interface device. If the signal SOH_disable is inactive, the counter AWC activates a signal write_enable. At the same time, the counter AWC is incremented by the number of incoming payload bytes. The value obtained in this manner is supplied to the circular buffer R via a signal addr_in and is interpreted as address by the buffer. The data data_in are deposited in the circular buffer R as determined by this address. Due to the logical OR operation on the signals SOH_disable, POH_disable (write_enable), only payload is transferred into the circular buffer R. The information stored in the control fields SOH, POH is thus suppressed.

On start-up, the signals POH_J_1 of all interface devices $P_0...P_3$ are set to "0". If the signaling signal for the marker J_1 of the relevant interface device is detected, the counter PC is started by the signal POH_disable. The signal POH_J_1 of the corresponding interface device is then set to a logical "1" or "high". As long as the signal POH_J_1 assumes the state of logical "1", the payload bytes are counted. If the markers J_1 have been received by all interface devices $P_0...P_3$, all signals POH_J_1 are then set to a logical "1". As a result, the monitoring device PD initiates logic operations and forms the difference between the counts AWC and PC, decremented by 1 and loaded into the counter ARC. The monitoring device PD then sets all signals POH_J_1 to 0 for the next cycle. Furthermore, if the counts of the counters AWC and ARC are equal, the read process is stopped in all interface devices and a signal disable_read is generated because there is no payload in the circular buffer R

in at least one of the interface devices $P_0 \ldots P_3$.

In detail, the following procedure is adopted:

The counts of counters AWC and PC are determined. The difference between the two counts is decremented by 1 and the result is stored in the counter ARC. At the instant at which all markers J_1 have arrived, the relative delay difference of the STM-1 signals with respect to the STM-1 signals which have arrived last is thus given in the counter PC.

The counters ARC of all interface devices are then triggered to transfer the content to the circular buffer R via in each case one signal addr_out. The latter interprets this value as an address. The data stored under this address are read out and forwarded as STM-4 signal as output data data_out.

The corresponding conditions are reproduced in figure 4. Accordingly, the 4 cyclic circular buffers R of the 4 interface devices $R(P_0) \ldots R(P_3)$ are shown. As a last marker, marker J_1 of the interface devices P_1 has arrived, for example. All counters are then stopped. Subsequently, the relative address to the markers J_1 which are stored in the remaining 3 interface devices is then formed. In the case of the interface devices $R(P_0)$ the difference is 6 payload bytes. In the case of the interface device P_2, the difference is 8 payload bytes and in the case of the interface device P_3, the difference is 17 payload bytes. Triggering the higher-level logic device RC, the payload is read out and supplied to an STM-4 frame FR which regenerates 1 STM-4 signal from the 4 STM-1 signals.

The precondition for this method is that the markers J_1 of all STM-1 signals arrive within a half VC-4 period. The corresponding conditions are shown for the example of 4 STM-1 signals in figure 2. The markers J_1 are placed within the VC-4 period. For this reason, the interface circuits can synchronize without additional signal evaluation. For example, marker J_1 of frame F_3 of interface device P_3 arrives first, for example, as described for figure 2. The counter PC is then started and counts up to 1170. If no further markers J_1 of the remaining containers CON are detected until then, all counters PC and all signals POH_J_1 are reset and synchronization recommences correctly with marker J_1 of frame F_1 at the next cycle.

According to the present exemplary embodiment, it has been assumed that the magnitude of the delay differences is smaller than one half container period of a virtual VC-4 container. However, delay differences greater than one half container period of a virtual VC-4 container can also be treated with a modification of the method.

The interface device according to figure 3 can still synchronize if the payload in the container is structured. In this case, the circular buffer R must be enlarged in accordance with the greatest delay to be expected. The corresponding conditions are shown in figure 5. This is the case, for example, if the payload consists of ATM cells, frame relay or TCP/IP data. Because of such transmission formats, synchronization can be carried out because error-free transmission is detected by the control field SOH and in this case the header of the cell is detected and evaluated by an additional payload synchronization circuit corresponding to the transmission format. The synchronization circuit is designated by HSC in figure 5. The synchronization can be restored by

combining the pointers of 2 or more VC-4 containers (4 pointers in the case of STM-4) until the payload synchronization circuit HSC acquires lock. The combination can be obtained from a simple addition of 2340 bytes in the counting devices of the counters ARC - triggered by a device J_1CL (J_1 combining logic) since, when a number of markers J_1 is found, the frame to which this marker belongs cannot be reliably detected. The difference between 2 markers J_1 of the same interface device is 2340 payload bytes. After the payload synchronization circuit HSC has acquired lock, the markers J_1 will not be combined because only jumps of 3 bytes are allowed according to the SDH standard, unless the system is re-initialized.

Patent claims

1. A method for converting NxSTM-1 signals into STM-N signals, comprising

a multiplicity (N) of STM-1 signals (data_in0...data_inN) which in each case have a first and second control field (SOH, POH) and a payload field (CON) filled with payload, the beginning of which is defined by a marker (J_1) and comprising a multiplicity (N) of interface devices ($P_0...P_N$) which in each case have a store (R) and which are used for accommodating the multiplicity (N) of STM-1 signals (data_in0...data_inN),

characterized in that

the payload of the multiplicity (N) of STM-1 signals is stored in a cyclic order in the store (R) of the in each case associated interface device ($P_0...P_N$) at a write address corresponding to the number of payload data which have arrived,

a relative address is formed with respect to the markers (J_1) which have arrived until then, on the basis of the marker (J_1) which has arrived last, and

at the relative address formed in this manner, the payload is removed again from the stores (R) of the in each case associated interface device ($P_0...P_N$) in the same cyclic order as during the write process and is supplied to an STM-N frame (FR) as output data (data_out0...data_outN).

2. The method as claimed in claim 1,

characterized in that,

the write address in the store (R) is formed by incrementing in a first counting device (AWC) as determined by the number of payload data that have arrived, until the first control field (SOH) or the second control field (POH) is detected, and the count of the first counting device (AWC) is transferred to the store (R).

3. The method as claimed in claim 1, characterized in that, the payload data are counted in a second counting device (PC) from the instant where the second control field (POH) is detected until the time where all markers (J_1) have arrived, and then the difference between the counts of the first and second counting device (AWC, PC) is formed, which is further decremented by 1, and the value calculated in this manner is transferred as read address to a third counting device (ARC) at which the payload stored in the store (R) is removed.

4. The method as claimed in one of claims 1 to 3, characterized in that, the store (R) is constructed as a cyclic random-access circular buffer.

5. The method as claimed in one of claims 1 to 4, characterized in that, the interface devices ($P_0 \ldots P_N$) are synchronized within one half period of a VC-4 container (CON).

6. The method as claimed in one of claims 1 to 4, characterized in that, the interface devices ($P_0 \ldots P_N$) are synchronized outside the half period of a VC-4 container (CON) by combining the pointers of at least two VC-4 containers until a synchronization circuit (HSC) which follows the interface devices ($P_0 \ldots P_N$) and determines structured payload data acquires lock.

GR 99 P 1120

Abstract

Method for converting NxSTM-1 signals into STM-N signals

During the transmission of SDH signals, higher-order signals such as STM-N (N>1) signals are transmitted. To prevent circuit switching problems in the STM-1 switching networks hitherto used, the STM-N signals are split into N STM-1 signals in accordance with the known virtual concatenation mode. These signals, however, pass through different paths in the network which leads to different delays. The invention solves these problems by addressing FIFO storage devices with relative addressing at the receiving end in order to read out the payload data stored there.

Figure 3

BOX PCT

IN THE UNITED STATES ELECTED/DESIGNATED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY-CHAPTER II

SUBMISSION OF DRAWINGS

APPLICANT:	Athanase Mariggis	DOCKET NO: 112740-219
SERIAL NO:		GROUP ART UNIT:
		EXAMINER:
INTERNATIONAL APPLICATION NO:		PCT/DE00/00176
INTERNATIONAL FILING DATE:		21 January 2000
INVENTION:	METHOD FOR CONVERTING NxSTM-1 SIGNALS INTO STM-N SIGNALS	

Assistant Commissioner for Patents,
Washington, D.C. 20231

Sir:

Applicant herewith submits five sheets (Figs. 1-5) of drawings for the above-referenced PCT application.

Respectfully submitted,

(Reg. No. 39,056)

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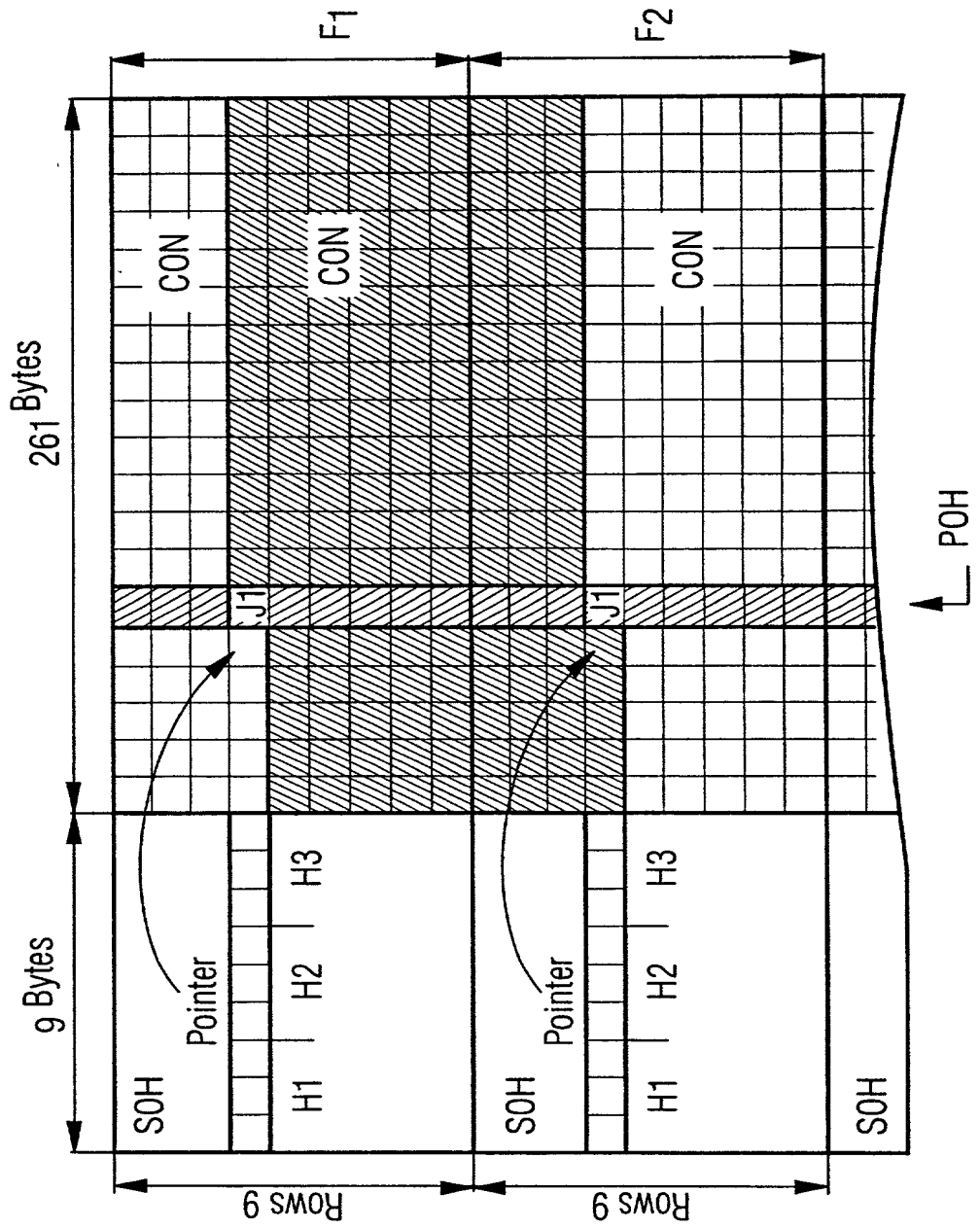

F1
F2
261 Bytes
9 Bytes
CON
CON
CON
J1
J1
POH
Pointer
Pointer
H3
H2
H1
H3
H2
H1
SOH
SOH
SOH
Rows 9
Rows 9

FIG 1

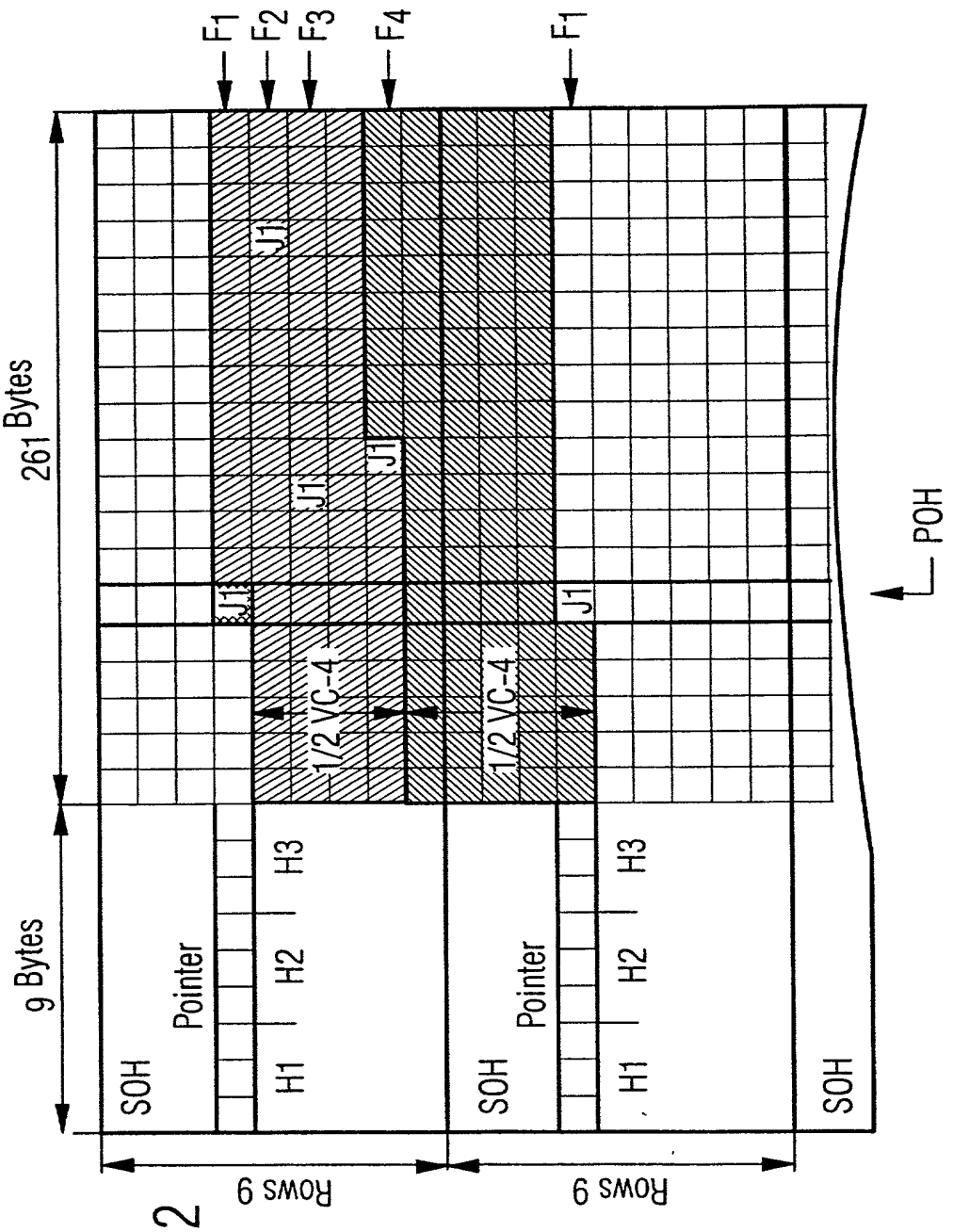
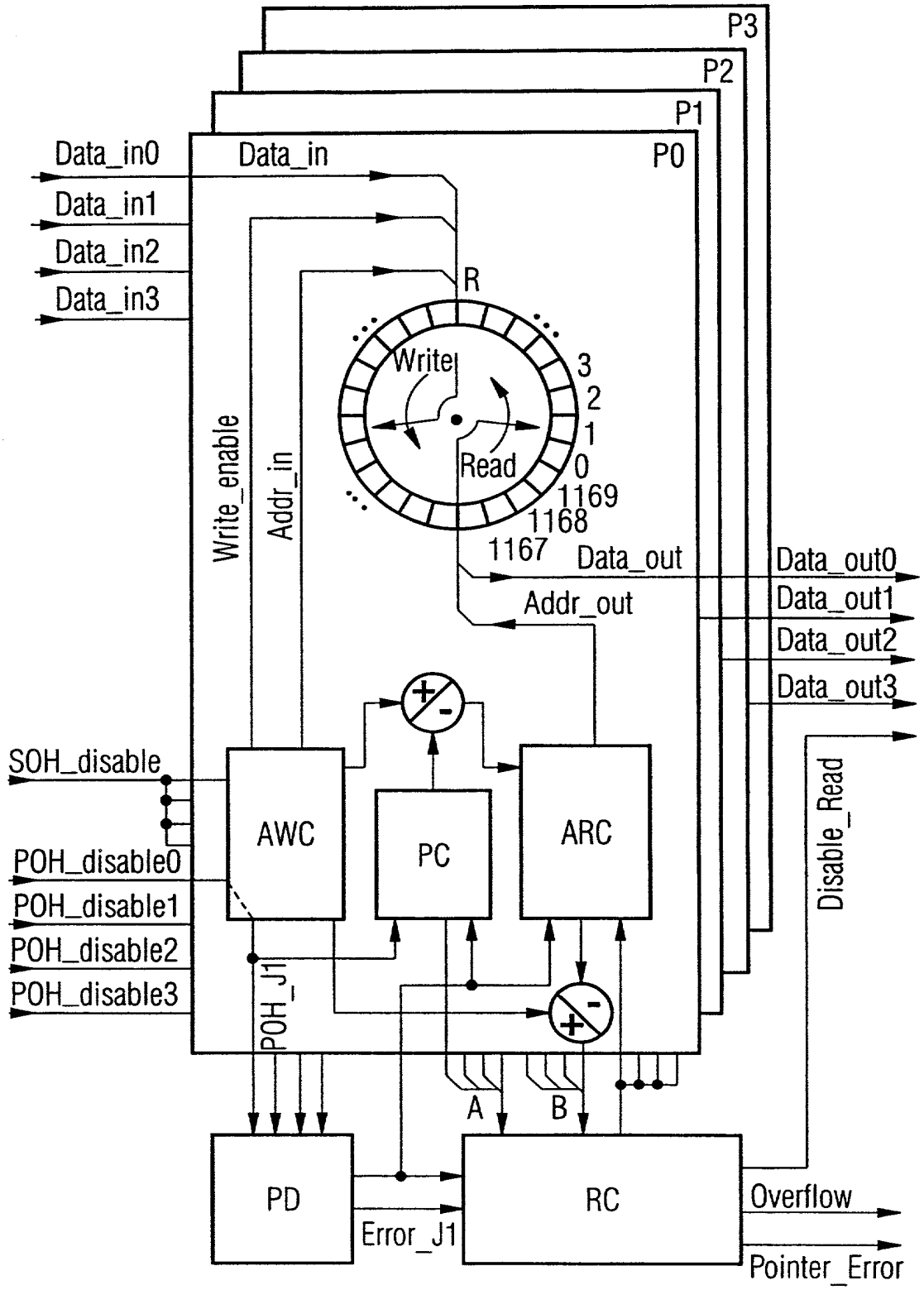

F1
F2
F3
F4
F1
261 Bytes
9 Bytes
J1
J1
J1
J1
J1
1/2 VC-4
1/2 VC-4
POH
SOH
Pointer
H1
H2
H3
SOH
Pointer
H1
H2
H3
SOH
Rows 9
Rows 9

FIG 2

FIG 3


P3
P2
P1
P0
Data_in0
Data_in1
Data_in2
Data_in3
Data_in
R
Write
Read
3
2
1
0
1169
1168
1167
Write_enable
Addr_in
Data_out
Addr_out
Data_out0
Data_out1
Data_out2
Data_out3
SOH_disable
POH_disable0
POH_disable1
POH_disable2
POH_disable3
AWC
PC
ARC
POH_J1
A
B
Disable_Read
PD
RC
Error_J1
Overflow
Pointer_Error

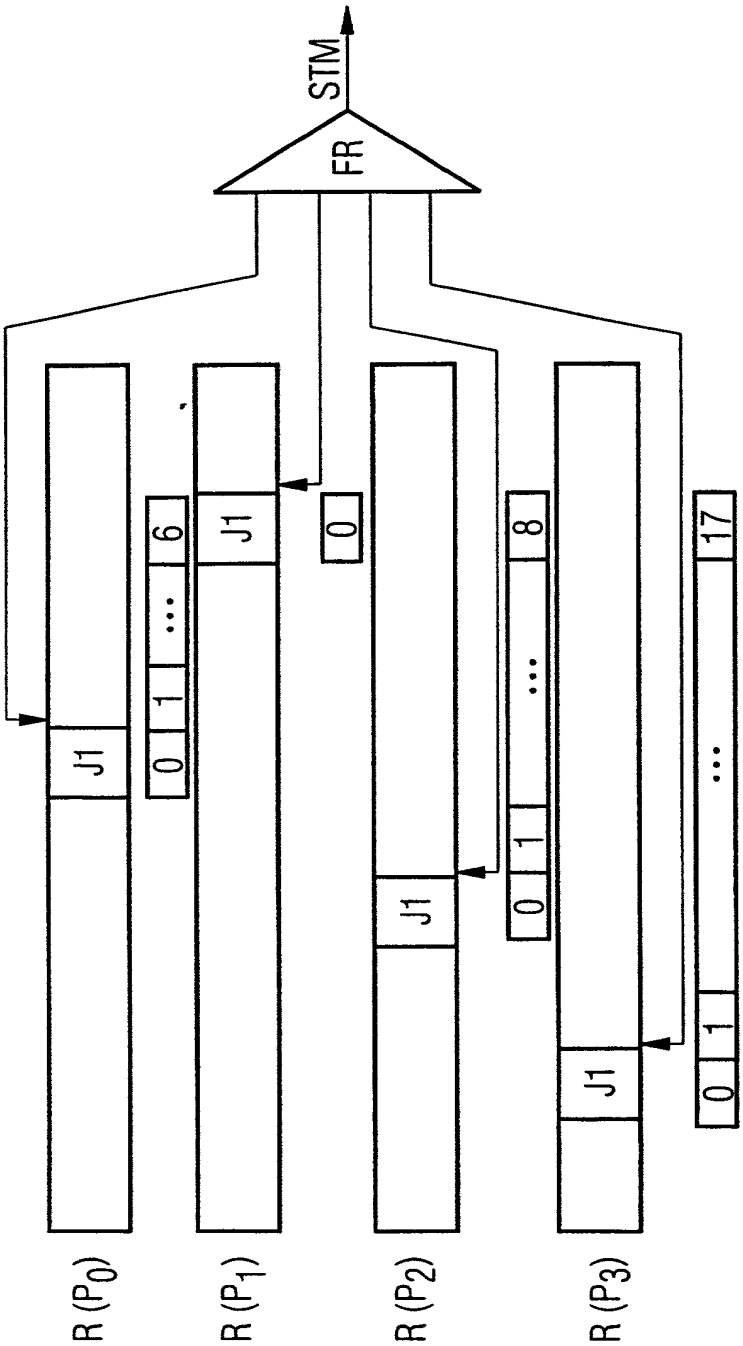
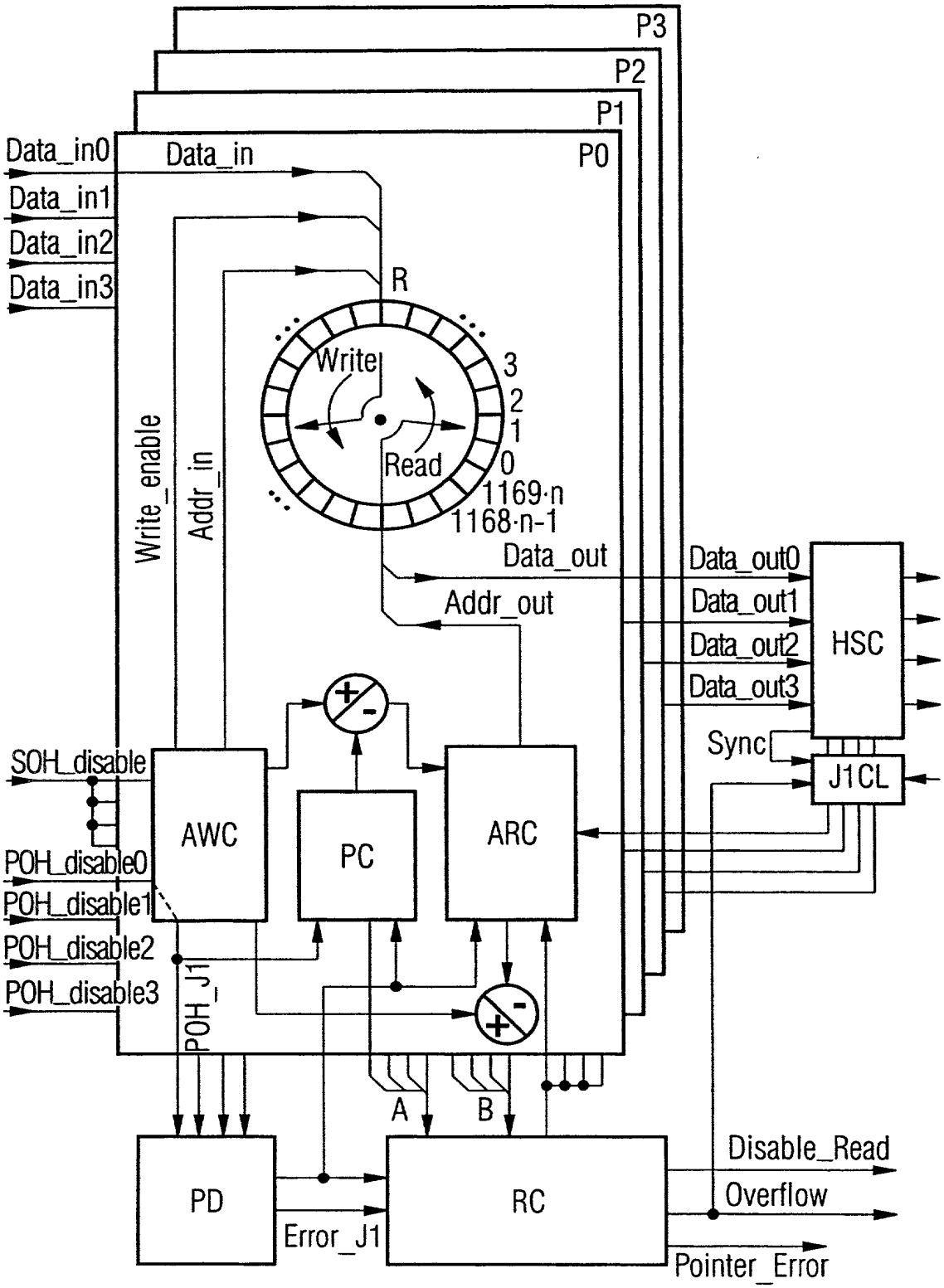


FIG 4

FIG 5


P3
P2
P1
P0
Data_in0
Data_in1
Data_in2
Data_in3
Data_in
R
Write
Read
3
2
1
0
1169·n
1168·n-1
Write_enable
Addr_in
Data_out
Addr_out
Data_out0
Data_out1
Data_out2
Data_out3
HSC
Sync
J1CL
SOH_disable
POH_disable0
POH_disable1
POH_disable2
POH_disable3
AWC
PC
ARC
POH_J1
A
B
PD
RC
Error_J1
Disable_Read
Overflow
Pointer_Error

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

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Verfahren zum Umsetzen von NxSTM-1 Signalen in STM-N Signale

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 21.01.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/00176
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

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As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method for converting NxSTM-1 signals into STM-N signals

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 21.01.2000 as
PCT international application
PCT Application No. PCT/DE00/00176
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications Priorität beansprucht			Priority Claimed	
19903366.8 (Number) (Nummer)	DE (Country) (Land)	28.01.1999 (Day Month Year Filed) (Tag Monat Jahr eingereicht)	☒ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/00176 (Application Serial No.) (Anmeldeseriennummer)	21.01.2000 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	_____ (Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
_____ (Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	_____ (Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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17

Holby M. Abern (P47,372), Robert M. Barrett (30,142), Alan L. Barry (30,819), Thomas C. Basso (46,541), Jeffrey H. Canfield (38,404), Robert W. Connors (46,639), Amy J. Gast (41,773), Timothy L. Harney (38,174), Patricia A. Kane (46,446), Michael S. Leonard (37,557), Edward A. Lehman (22,312), Adam H. Masia (35,602), Dante J. Picciano (33,543), Renato L. Smith (45,117), Maurice E. Teixeira (45,646), William E. Vaughan (39,056), Austin Victor (47,154), and all members of the firm of Bell, Boyd & Lloyd LLC.

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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~~70 West Madison Street, Suite 3300 60602-4207~~ Chicago, Illinois
Telephone: +1 312 372 1121 and Facsimile +1 312 372 2098
or
Customer No.

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
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Unterschrift des Erfinders Datum: Athanase Mariggis (Mariggis) 9.5.2001	Inventor's signature Date
Wohnsitz: MUENCHEN, DEUTSCHLAND	Residence: MUENCHEN, GERMANY
~~Staatsangehörigkeit~~: DE	Citizenship: DE
Postanschrift: SCHUCKERSTR. 1 81379 MUENCHEN	Post Office Addess: SCHUCKERSTR. 1 81379 MUENCHEN
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).